

App. No. 10/657,393
Amendment Dated December 20, 2004
Reply to Office Action of September 20, 2004

Listing of claims:

1. (Original) A switching regulator that is arranged to provide current to a load circuit, comprising:

a first resistor that is coupled between a first node and a second node, wherein the first node is associated with an input voltage;

a second resistor that is coupled between the second node and a circuit ground;

an inductor that is coupled between the first node and a third node;

a third resistor that is coupled between the third node and a fourth node;

a fourth resistor that is coupled between the fourth node and the circuit ground;

a diode that is coupled between the third node and the load circuit;

a capacitor that is coupled in parallel with the load circuit;

a switch circuit that is arranged to selectively couple the third node to the circuit ground in response to a pulsed gate signal; and

a voltage controlled oscillator that is responsive to a frequency signal from the third node and arranged to provide a pulsed gate signal, wherein the voltage controlled oscillator is: disabled by a first signal from the fourth node when the first signal is above a predetermined reference level, enabled when the first signal is below the predetermined reference level, and arranged to provide the pulsed gate signal when enabled such that the switch circuit is activated for a time interval that is associated with a pulse width that is determined by a second signal from the second node.

2. (Original) The switching regulator of Claim 1, wherein the voltage controlled oscillator is arranged to adjust the pulse width by sensing a second voltage that is associated with the second signal, where the second voltage is related to the input voltage according to a voltage divider that is formed by the first and second resistors.

3. (Original) The switching regulator of Claim 1, wherein the voltage controlled oscillator is arranged to adjust the pulse width by sensing a second current that is associated with the second signal, where the second current is related to the input voltage by a first value that is associated with the first resistor.

App. No. 10/657,393

Amendment Dated December 20, 2004

Reply to Office Action of September 20, 2004

4. (Original) The switching regulator of Claim 1, wherein the first signal corresponds to a first voltage that is provided by a voltage divider that is formed by the third and fourth resistors.

5. (Original) The switching regulator of Claim 1, further comprising a comparator circuit that is arranged to disable the voltage controlled oscillator when the first signal exceeds the predetermined reference level.

6. (Original) The switching regulator of Claim 1, wherein the predetermined reference level corresponds to a band-gap voltage.

7. (Original) The switching regulator of Claim 1, wherein a third voltage associated with the third node: corresponds to a ground potential when the switch circuit is activated, is related to the output voltage when the switch circuit is deactivated and the inductor is discharging, and collapses towards the ground potential when the inductor is discharged.

8. (Original) The switching regulator of Claim 7, wherein the first signal corresponds to a scaled version of the third voltage, where a scaling factor associated with the scaled version is determined by the third and fourth resistors.

9. (Original) The switching regulator of Claim 1, wherein the diode is a Schottky-type diode.

10. (Original) The switching regulator of Claim 1, wherein the load circuit comprises an array of light emitting diodes that are coupled together to operate as a constant voltage load.

11. (Currently Amended) A switching regulator that is arranged to generate an output voltage (V_{OUT}) from an input voltage (V_{IN}) by coupling a current (I_{LOAD}) to a load circuit, the switching regulator comprising:

an inductor that is coupled between a first node and a second node, wherein the first node is associated with the input voltage, wherein the inductor has a value that corresponds to L ;

a diode that is coupled between the second node and the load circuit;

a sense means that is arranged to monitor a sense voltage from the second node;

an oscillator means that is arranged to selectively provide a gate signal when enabled, wherein a pulse width associated with the gate signal is responsive to the input voltage (V_{IN});

App. No. 10/657,393
Amendment Dated December 20, 2004
Reply to Office Action of September 20, 2004

a switch means that is arranged to selectively couple the ~~third~~ second node to a circuit ground when the gate signal is asserted; and

a disable means that is arranged to disable the oscillator means in response to the sense voltage when the inductor is discharging until the sense voltage collapses below a predetermined reference level such that the switching regulator is operated in a discontinuous current mode.

12. (Original) The switching regulator of Claim 11, wherein the switching regulator is arranged such that an off-time (T_{OFF}) and an on-time (T_{ON}) associated with the switch means are linearly related to one another according to: $T_{OFF} = T_{ON} * V_{IN} / (V_{OUT} - V_{IN})$.

13. (Original) The switching regulator of Claim 11, wherein the switching regulator is arranged such that a period associated with the switching regulator is determined by: $\text{Period} = T_{ON} * V_{OUT} / (V_{OUT} - V_{IN})$, wherein T_{ON} is associated with the pulsed gate signal.

14. (Original) The switching regulator of Claim 11, wherein the switching regulator is arranged such that the current (I_{LOAD}) that is provided to the load circuit is given by: $I_{LOAD} = (K / 2L) * (V_{IN}^2 / V_{OUT}) / (V_{IN} - X)$, where K is a constant and X is an intercept value associated with a linear relationship between pulse width and input voltage.

15. (Original) The switching regulator of Claim 11, wherein the switching regulator is arranged such that the pulse width of the gate signal linearly decreases with increased values of input voltage.

16. (Original) The switching regulator of Claim 11, wherein the switching regulator is arranged such that decreases in the pulse width reduces power consumption of the switching regulator at the same rate that the input voltage increases such that the switching regulator operates as a constant power output circuit.

17. (Currently Amended) A method of generating an output voltage (V_{OUT}) for a load circuit from an input voltage (V_{IN}) with a switching regulator, the method comprising:

coupling an inductor to a circuit ground such that the inductor is charged during a first cycle, wherein the inductor has a value corresponding to L ;

App. No. 10/657,393

Amendment Dated December 20, 2004

Reply to Office Action of September 20, 2004

discharging the inductor after the first cycle by coupling energy from the inductor to the load circuit through a diode during a second cycle, wherein the second cycle is different from the first cycle;

sensing when the inductor is discharged;

restarting the first cycle when the inductor is determined to be discharged such that the switching regulator is operated in a discontinuous current mode; and

adjusting the period associated with the first cycle in response to the input voltage (V_{IN}) such that a load current that is provided to the load circuit is a linear function of the input voltage (V_{IN}).

18. (Original) The method of Claim 17, wherein sensing when the inductor is discharged corresponds to: monitoring a voltage associated with the inductor to determine when the inductor is discharged, and comparing the monitored voltage to a predetermined reference level.

19. (Original) The method of Claim 17, wherein adjusting the period associated with the first cycle comprises: linearly decreasing the period associated with the first cycle when the input voltage increases, and linearly increasing the period associated with the first cycle when the input voltage decreases.

20. (Original) The method of Claim 17, further comprising: adjusting a current (I_{LOAD}) that is provided to the load circuit according to: $I_{LOAD} = (K/2L) * (V_{in}^2/V_o) / (V_{in} - X)$, where K is a constant and X is an intercept value associated with a linear relationship between pulse width and input voltage.